Ramya Prasanthi Kota, Nagaraja Kumar Pateti, Dr.Ch.D. V. Paradesi Rao/International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 1, Issue 3, pp.884-890

Algorithm to detect the proximity of a Moving Target & its Implementation on FPGA

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Abstract—

This paper presents an algorithm to detect the proximity of a target. The present work totally relates to a Radar System. Speed and accuracy are the two important factors to be considered. The challenges in developing the algorithm is to detect the target even if it is approaching closer to our Radar within a specified range (0 to 45 mts) with a range resolution of 3mts.

Keywords— Radar, Range, Range Resolution, BPSK Modulation, Pseudo Random Binary Sequence, Correlation, Digital Correlator, Vertex-4 (XC4VSX35-10ff668) FPGA.

I INTRODUCTION

Radar is derived from the initials of the phrase **RAdio Detection And Ranging**. Radar is an electromagnetic system used for the detection and location of objects (or targets). It achieves these two purposes by transmitting an electromagnetic energy and then extracting the necessary information about the target from the returned echo. This information is drawn from the changes observed in the signal parameters. The range, or distance, is determined from the measurements of the time taken for the radar signal to travel to the target and back (time delay). Radar measurement of range, or distance, is made possible because of the properties of radiated electromagnetic energy.

1. **Reflection of electromagnetic waves**
   The electromagnetic waves are reflected if they meet an electrically leading surface. If these reflected waves are received again at the place of their origin, then that means an obstacle is in the propagation direction.
2. Electromagnetic energy travels through air at a constant speed, at approximately the speed of light,
   - 300,000 kilometres per second or
   - 186,000 statute miles per second or
   - 162,000 nautical miles per second.

This constant speed allows the determination of the distance between the reflecting objects (airplanes, ships or cars) and the radar site by measuring the running time of the transmitted pulses.
These principles can basically be implemented in a radar system, and allow the determination of the distance, the direction and the height of the reflecting object. The ability to determine range by measuring the time for the radar signal to propagate to the target and back is probably the distinguishing and most important characteristic of conventional radar.

This paper describes a new algorithm to detect the closeness of a target within specified range within short period of time. The proposed method uses BPSK Modulation Scheme using Maximal Length Pseudo Random Binary Sequence.

II PSEUDO RANDOM BINARY SEQUENCE

PRBS or pseudo random binary sequence is essentially a random sequence of binary numbers. It is random in the sense that the value of an element of that sequence is independent of values of any other elements. It is pseudo because it is deterministic and after N elements it starts to repeat itself unlike real random numbers. Examples of random sequence are radioactive decay and white noise.
A binary sequence is a sequence of N bits, aj for j=0, 1, 2, --- N-1 i.e., m ones and N-m zeroes. A binary sequence is pseudo random if their auto correlations function:

$$C(v) = \sum_{j=0}^{N-1} (a_j a_{j+v})$$

Which has only two values i.e.,
C (v) =m if v=0(mod N)
C (v) =mc if v≠0 (mod N)
Where
C= (m-1)/ (N-1) which is called as the duty cycle of PRBS.
PRBS can be generated using **Linear Feed Back Shift Registers (LFSR).**

CHARACTERISTICS OF MAXIMAL LENGTH TAP SEQUENCES:

Period of an LFSR is the length of the output stream before it repeats. Besides being non repetitive, a period of maximal length stream has other features that are characteristics of random streams.

1. **Sums of ones and zeroes**
   In one period of a maximal length stream, the sum of all ones will be one greater than the sum of all zeroes.

2. If the length of sequence is N= 2^{m-1} where m is number of shift register stages, then it is maximal length sequence otherwise non-maximal length sequence.

3. **Runs of ones and zeros**
   A run is a pattern of equal values in the bit stream. One period of an n bit LFSR with a maximal length tap sequence will have 2^{n-1} runs. For example a 5 bit device yields 16 runs in one period. ½ the runs will be one bit long , 1/4 the runs will be 2 bits long, 1/8 the runs will be 3 bits long etc., up to a single run of zeros that is n-1 bits long and a single run of ones that is n bits long.

4. **Shifted stream**
   Take the stream of bits in one period of an LFSR with a maximal length tap sequence and circularly shift it any number of bits less than the total length. Do a bit wise xor with the original stream. It is another replica of same with a shift different from either one.

   In this sequence is generated wrt 10MHz i.e., 100ns clock with a period of 3.1micro seconds.

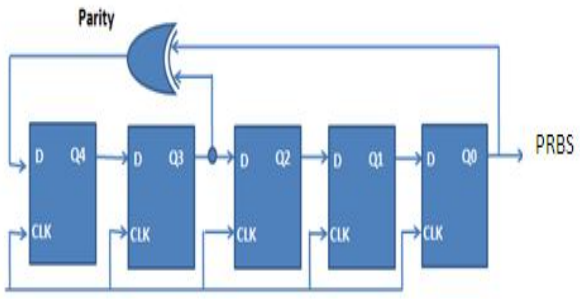


Figure 1: PRBS

III BINARY PHASE SHIFT KEY

(BPSK MODULATION)

Binary data are represented by two signals with different phases in BPSK. Typically these two phases are 0 and π, the signals are

$S_1(t) = A\cos 2\pi f_c t$, $0 \le t \le T$, for 1

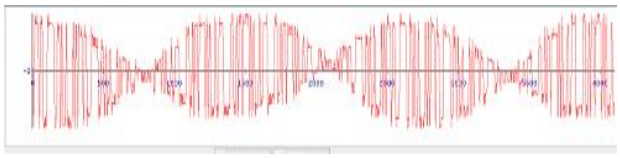
$S_2(t) = -A\cos 2\pi f_c t$, $0 \le t \le T$, for 0

These signals are called *antipodal*. The reason that they are chosen is that they have a correlation coefficient of −1, which leads to the minimum error probability for the same E_b/No. These two signals have the same frequency and energy.

The Radio frequency Signal transmitted undergoes BPSK modulation wrt the PRBS generated and it is returned back when it hits a target. As the signal travels some distance, the received signal will be exactly the same as the delayed version of the transmitted PN sequence. The received signal is down converted to IF signal in the mixer The IF signal has purely the information about range.

IV RECEIVED SIGNAL

The received IF signal which is modulated with the PRBS undergoes time delay and Doppler shift. As the signal undergoes Doppler shift, it is difficult to extract the PRBS sequence. Generally Doppler amplitude appears maximum whenever received code matches with delayed transmitted code. So the received signal is passed through Analog to Digital converter and the extraction of PRBS is carried out as above.



V RANGE SIMULATOR

A range simulator has been designed which stores the delayed versions of the transmitted PRBS. The output from the range simulator is used as a reference input to the correlator. The range simulator is designed using Serial in Parallel out Shift Register. Here the delayed versions of the

PRBS are generated with 100MHz period i.e., 10ns delay

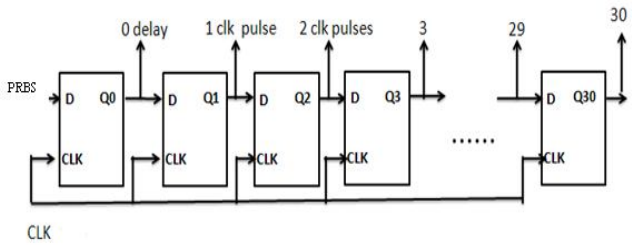


Figure 2: Serial in Parallel out Shifter

VI CORRELATION LOGIC

Correlation process is carried out for the Pseudo Random Binary sequence retrieved with the delayed versions of the reference sequence from the range simulator. It performs equivalence checking using XNOR operation of the both the inputs of the correlator and accumulate the number of matches. If the count is greater than the threshold then it is considered for peak detection. The threshold is set by loop back testing i.e., just by transmitting and receiving the PRBS alone and by performing the correlation. The maximum number of matches in this case is taken as threshold. The peak detected is valid when peak is continuously detected more than thrice. Then the delay is noted down and the closeness of the target to Radar is calculated.

ALGORITHM:

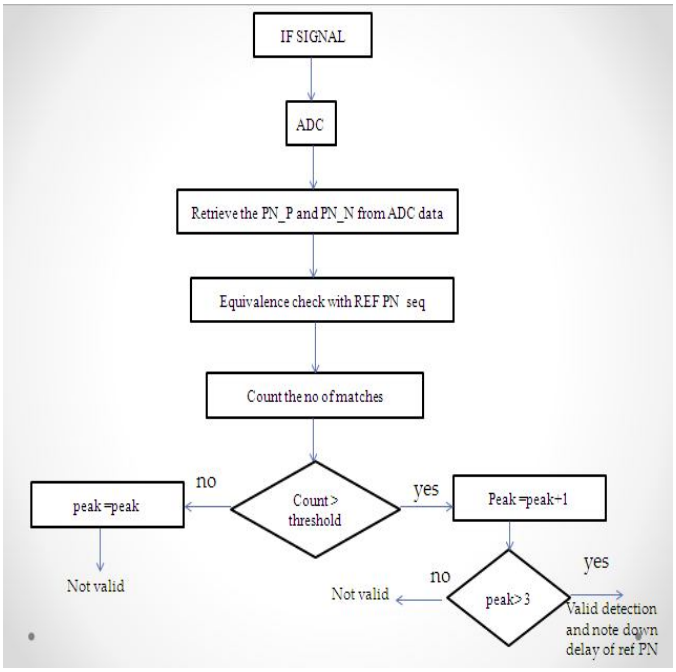
Explanation:

1. The received IF signal is passed through ADC.

2. Whenever the IF signal amplitude is maximum (i.e., higher than the threshold which is set by trial and error procedure), then PRBS bit of the received signal is 1 otherwise 0. This logic is used for retrieving the PRBS of the received signal.

3. The PRBS retrieved is digitally correlated (compare bit by bit and increment the number of matches) with the transmitted PRBS and also its delayed versions.
   The process is continued till the completion of one period. If the count is greater than the threshold considered, then it is taken as valid detection.

4. If this valid detection is observed more than thrice then the delay of the reference PRBS is noted down to calculate the range.



Flow chart for correlation logic

VII DIGITAL CORRELATOR

The digital correlator designed performs the correlation of the received PRBS with the delayed versions of the transmitted PRBS. This correlator has the capability of detecting target within the range of 45 mts with 3 mts resolution. So totally sixteen correlation logics are incorporated in the design and they perform their process parallely and the correlation logic with valid peak detection is taken and the delay of the reference PRBS of the respective logic is noted down to calculate range.

The figure 3 below illustrates the concept of digital correlation with five correlation logics i.e., correlation of received PRBS with five delayed versions of transmitted PRBS

Notation: T_x : Transmitted

T_{id} : (i*d) ns delayed version of Transmitted PRBS.

Where i=0 to 15 and d= 10ns delay

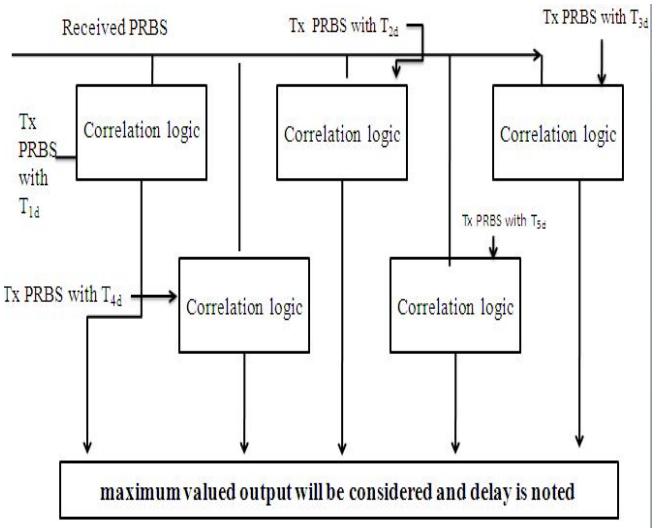


Figure 3: Block Diagram of Digital Correlator with five correlation logics.

VIII RANGE

The range can be calculated using the formula,

$$\text{Range} = c\frac{\tau}{2}$$

Where τ is the delay noted after digital correlation and c is the velocity of electromagnetic radiation.

IX SIMULATION RESULTS AND DISCUSSION

PRBS GENERATION:

The simulation shows the 31bit PRBS (PN_SEQ) generated wrt 10MHz clock i.e., 100ns with a period of 3.1 micro seconds.
Sequence generated is 1111100110100100001010111011000.

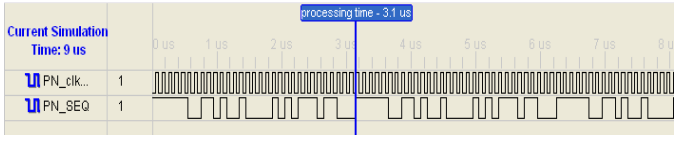


Figure 4: Simulation Results of PRBS generation

RANGE SIMULATOR:

Here SRL_IN is the PRBS generated and PN_REF is a 31 bit parallel data with each bit indicating the delayed versions of the generated PRBS wrt the clk.

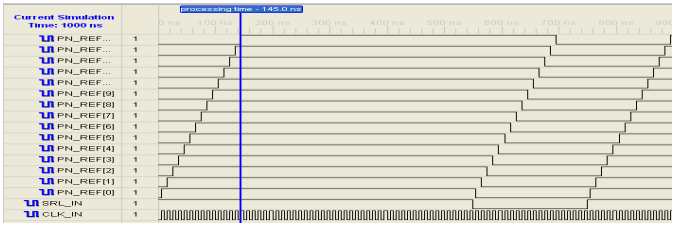


Figure 5: Delayed versions of transmitted PRBS

RECEIVED PRBS:

The received PRBS (PN_POS) shown is 280ns delayed version of transmitted PRBS (PN_SEQ) which is retrieved from ADC samples of IF signal.

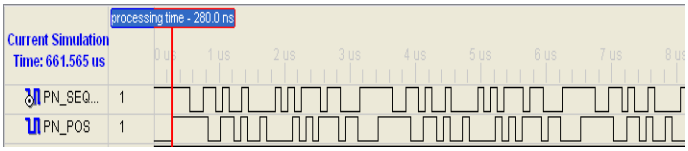


Figure 6: Received PRBS

CORRELATION LOGIC OUTPUT:

PN_P : Received PRBS
PN_REF : Reference PRBS from Range simulator
Compare1 : Equivalence checking (XNOR operation) of PN_P and PN_REF.

Sum1 : Counter logic accumulating the number of matches wrt W_CLK_100MHz.
CORR_VALID : Active high when sum1 reaches maximum Limit.
CORR_OUT : Identical to maximum value in sum1
PEAK : Counts the number of valid correlations

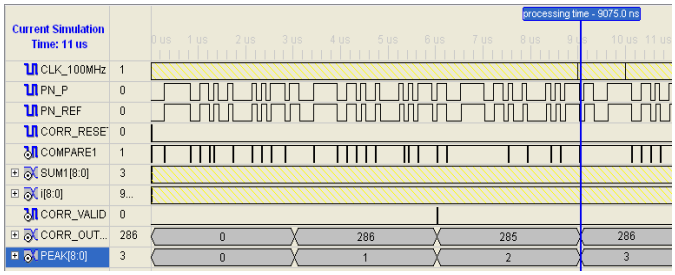


Figure 7: Correlation logic

RANGE ESTIMATION:

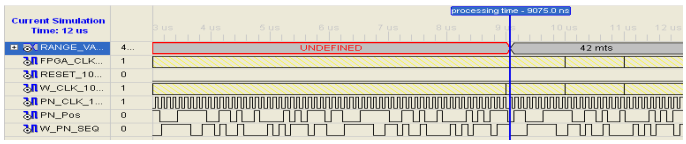


Figure 8: Range Estimator Output

X SYNTHESIS RESULTS

PRBS:

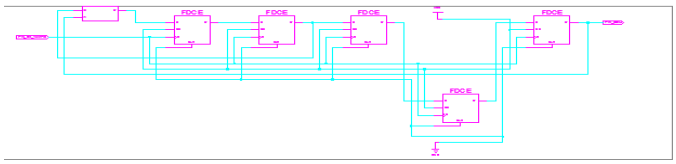


Figure 9: Pseudo Random Binary Sequence

RANGE SIMULATOR:

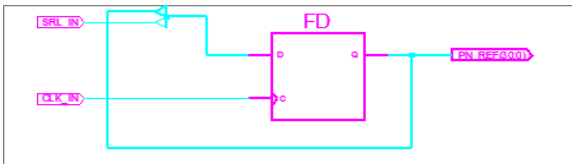


Figure 10: Range Simulator

DIGITAL CORRELATOR:

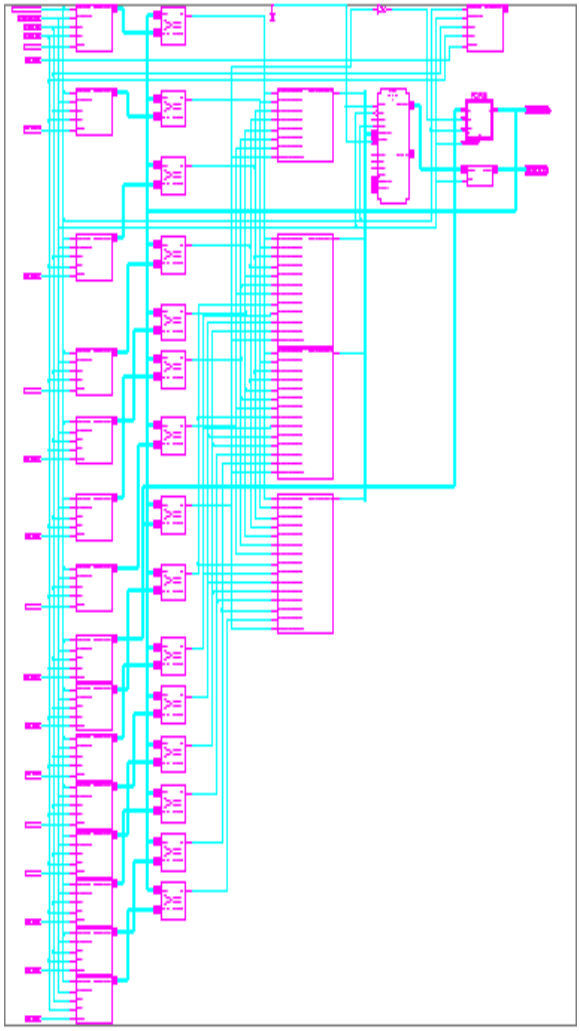
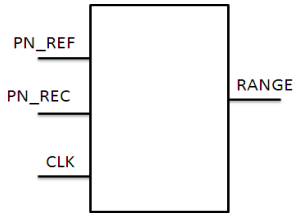


Figure 11: Digital Correlator

TOP MODULE:



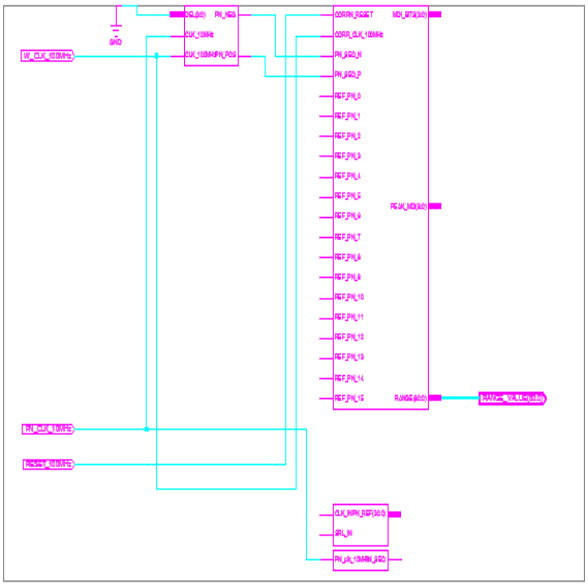


Figure 13: TOP MODULE INTERNAL VIEW

XI SYNTHESIS REPORTS

DEVICE UTILISATION SUMMARY:

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	1145	15360	7%
Number of Slice Flip Flops	846	30720	2%
Number of 4 input LUTs	2095	30720	6%
Number of bonded IOBs	88	448	19%
Number of FIFO16/RAMB16s	3	192	1%
Number of GCLKs	3	32	9%

Figure 14: Device Utilisation Summary

TIMING REPORT:

```
Speed Grade: -10

   Minimum period: 5.304ns (Maximum Frequency: 188.541MHz)
   Minimum input arrival time before clock: 4.974ns
   Maximum output required time after clock: 4.737ns
   Maximum combinational path delay: No path found
```

HDL SYNTHESIS REPORT:

```
HDL Synthesis Report

Macro Statistics
# ROMs                                  : 1
 16x81-bit ROM                         : 1
# Adders/Subtractors                    : 32
 9-bit adder                           : 32
# Counters                              : 64
 9-bit up counter                      : 64
# Registers                             : 54
 1-bit register                        : 18
 31-bit register                       : 2
 4-bit register                        : 1
 9-bit register                        : 33
# Latches                               : 1
 81-bit latch                          : 1
# Comparators                           : 63
 9-bit comparator greatequal           : 31
 9-bit comparator greater              : 16
 9-bit comparator less                 : 16
# Multiplexers                          : 2
 1-bit 16-to-1 multiplexer             : 2
# Xors                                  : 34
 1-bit xor2                            : 34
```

XII CONCLUSION

The algorithm was designed using Verilog coding and implemented in Xilinx Vertex 4 FPGA.By implementing this proposed technique, location of any object within 45mts can be found with a range resolution of 3mts. This particular algorithm can be implemented within a short span of time i.e., 9micro seconds. Even if the target is in motion it is not possible for the target to move more than 45 mts in any direction and hence the closeness can be detected easily.

ACKNOWLEDGMENT

We owe our sincere thanks to the academia of Aurora's Engineering College for permitting us to pursue the subject study. The technical guidance that we derived from Dr.Ch.D.V.Paradesi Rao enabled us to accomplish this task. And we owe our sincere thanks for the same. The presentation of this article could be a reality with the valuable technical input accorded from time to time.

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